



#2

04C0
01/19/01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: **U-Ming Ko**

Docket: **TI-29632**

Serial No.: **09/723,563**

Examiner: **TBD**

Filed: **11/28/2000**

Art Unit: **TBD**

For: **Input/Output Architecture for Integrated Circuits**

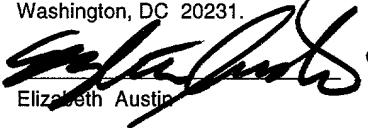
TRANSMITTAL OF FORMAL DRAWINGS

February 22, 2001

Assistant Commissioner For Patents

Attn: Official Drafts Person

Washington, DC 20231

<p>MAILING CERTIFICATE UNDER 37 C.F.R. § 1.8(a)</p> <p>I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner For Patents, Washington, DC 20231.</p> <p> 2/22/2001 Elizabeth Austin Date</p>

Dear Sir:

Submitted herewith are 5 sheets of formal drawings.

Respectfully submitted,



Texas Instruments Incorporated

Ronald O. Neerings

P. O. Box 655474, MS 3999

Attorney for Applicants

Dallas, Texas 75265

Reg. No.: 34,227

(972) 917-5299

Fax: (972) 917-4418

or (972) 917-4417

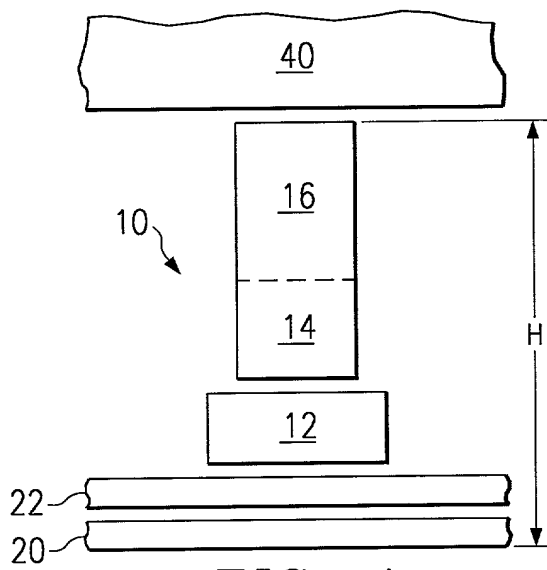


FIG. 1
(PRIOR ART)

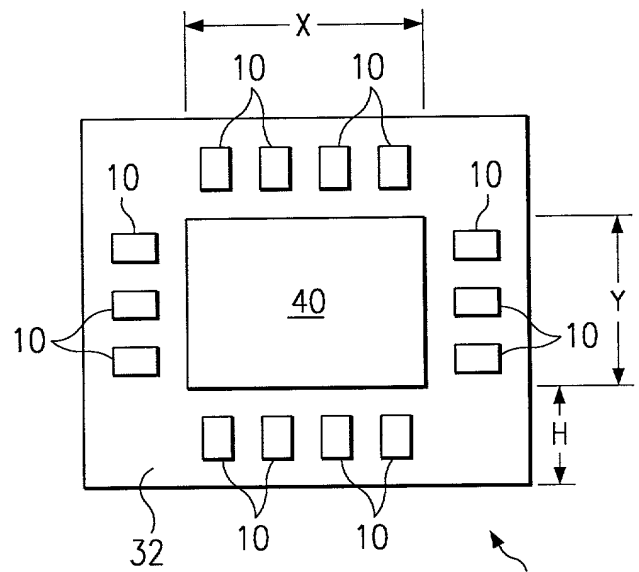


FIG. 2
(PRIOR ART)

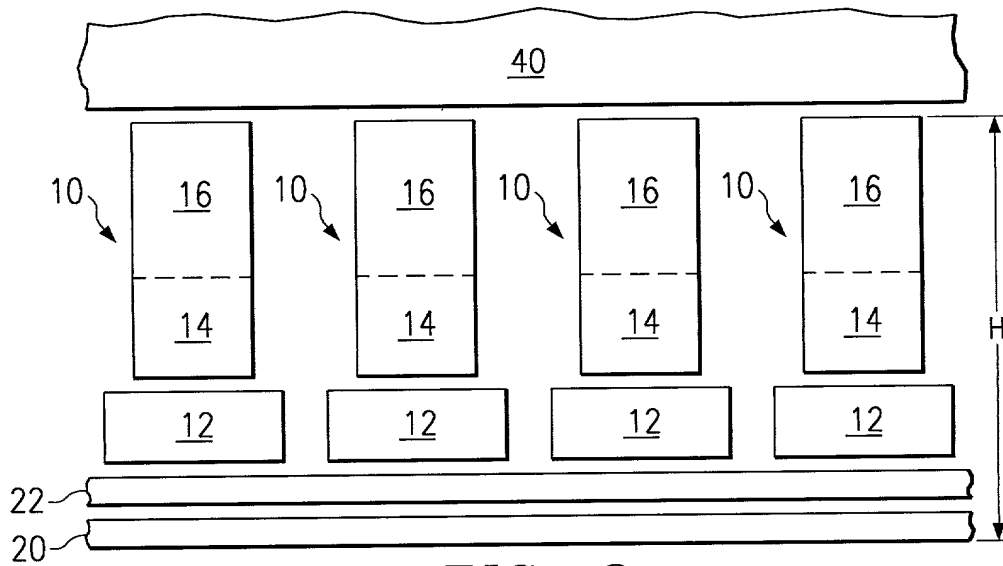


FIG. 3
(PRIOR ART)

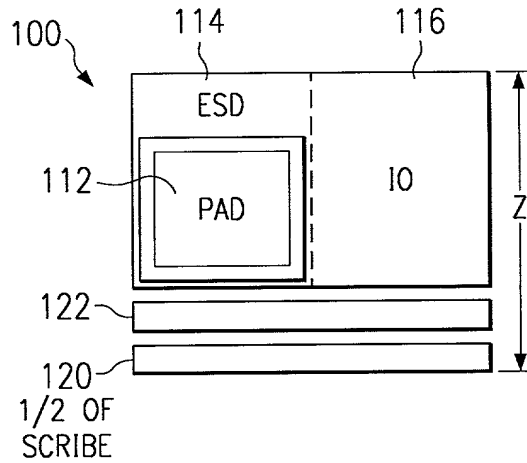


FIG. 4

FIG. 5

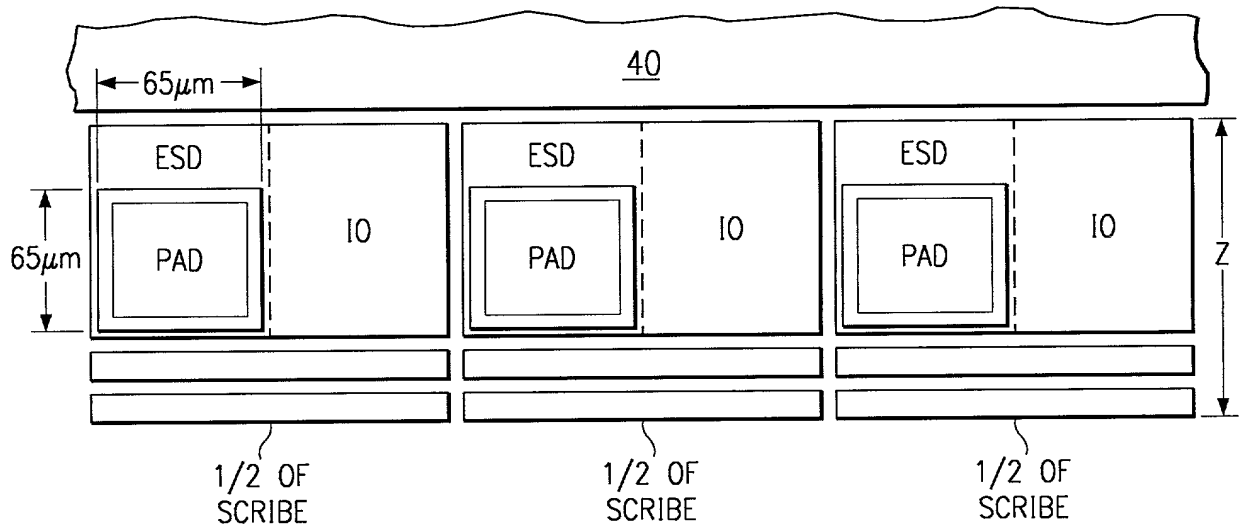


FIG. 6

CORE AREA, mm ²	mm/SIDE	IO HEIGHT, μm	IO WIDTH, μm	AREA	MAX IO	WASTED AREA	% OF CORE
10	3.162278	H=188	75	12.51941	169	1.67	13%
		Z=120	108	11.57549	117		
20	4.472136	H=188	75	23.50442	239	2.33	10%
		Z=120	108	22.20423	166		
30	5.477226	H=188	75	34.26025	292	2.83	8%
		Z=120	108	32.68667	203		
40	6.324555	H=188	75	44.89744	337	3.26	7%
		Z=120	108	43.09339	234		
50	7.071068	H=188	75	55.45882	377	3.63	7%
		Z=120	108	53.45171	262		
60	7.745967	H=188	75	65.96634	413	3.97	6%
		Z=120	108	63.77566	287		

FIG. 7

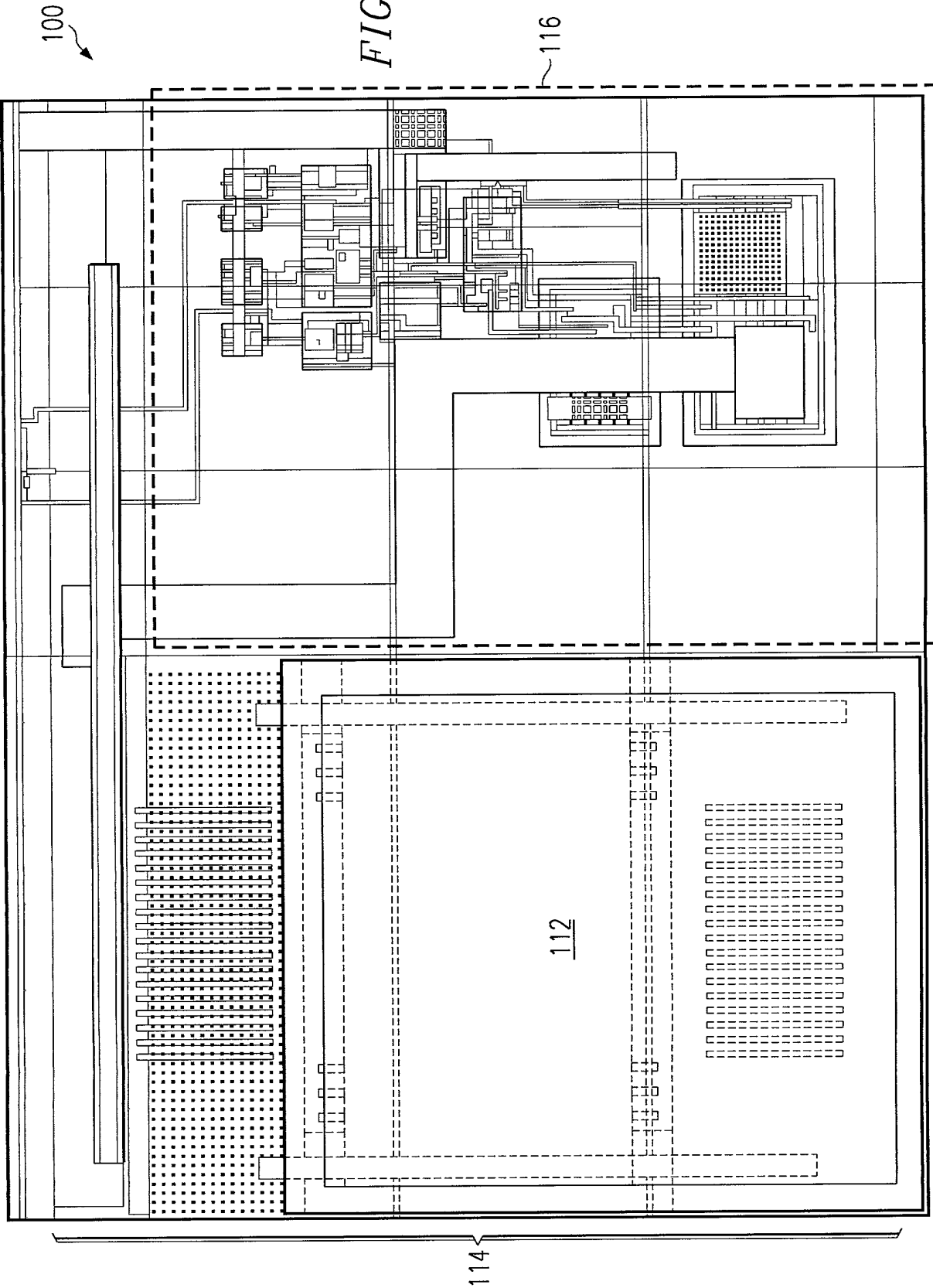




FIG. 9